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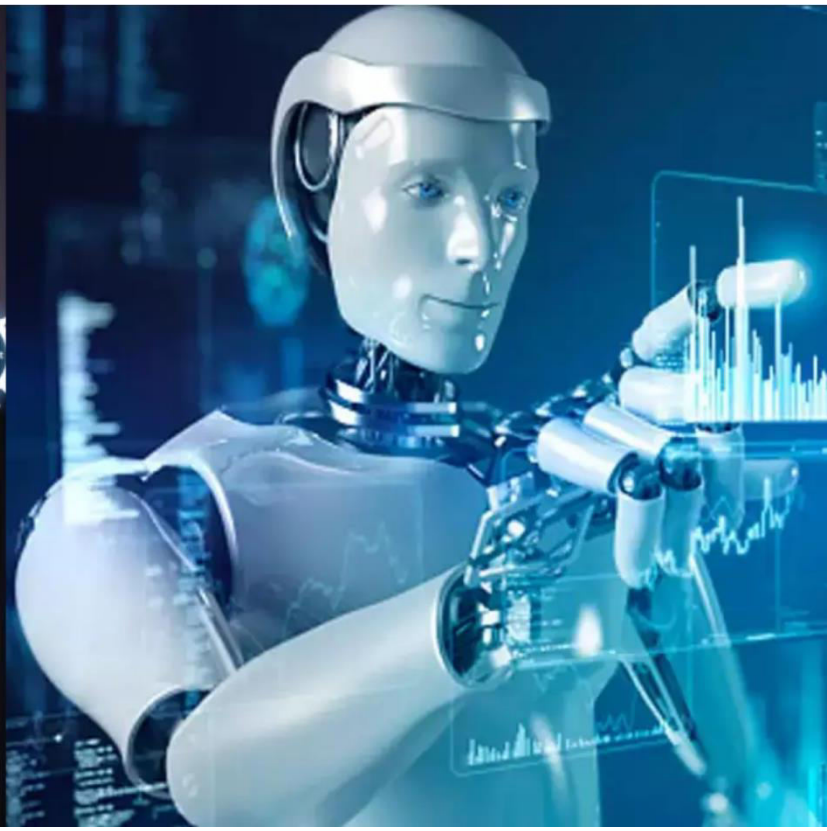

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Optimization of Layout Design in Integrated Circuits for Low-Power Applications: A Parasitic-Aware Study in 180 nm CMOS

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ABSTRACT: Dynamic power in mature CMOS nodes depends less on the transistors than on what surrounds them: diffusion area, wire length, and coupling between neighbouring metal tracks. This study examined how physical layout choices changed the power and delay of a 28-transistor mirror full adder built in 180 nm CMOS at a 1.8 V supply. We compared a conventional, hand-drawn layout with an optimized layout that combined Euler-path diffusion sharing, transistor folding, and short, metal-1-first routing. Both versions passed the same DRC and LVS checks and went through the same RC parasitic extraction flow. Post-layout transient simulation shows that parasitics raise the schematic's average power by about 22% and its worst-case delay by about 31%, so schematic-level numbers are too optimistic. The optimized layout recovered much of this loss. It cut the average power by 14.2% and propagation delay by 12.8% against the conventional layout at a cost of 3.1% extra cell area. For designs that cannot be moved to a finer node, careful layout remains one of the cheapest low-power techniques available.

KEYWORDS: CMOS Technology, VLSI Design, Low-Power Design, 180 nm CMOS, Parasitic Capacitance, Layout Optimization, Euler Path Diffusion Sharing, Power-Delay Product (PDP).

I. INTRODUCTION

Battery-powered electronics keep getting smaller, and their energy budgets keep shrinking with them. Sensor nodes, wearable monitors, and smart-meter chips often run for months on a coin cell; therefore, every microwatt matters. Many of these products use 180 nm CMOS. The node is cheap to fabricate and is tolerant of analog blocks, and a 1.8 V supply provides a comfortable noise margin.

At 180 nm, dynamic power dominates. Sub-threshold leakage is small, since threshold voltages sit near 0.45 V, so the familiar expression $P_{dyn} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f$ describes most of the consumption. Supply scaling is the usual first lever, but a 1.8 V rail with a 0.45 V threshold leaves little headroom before delay degrades sharply. That leaves the switched capacitance C_L, and layout decides most of it.

The layout sets the junction capacitance of every drain and source, length and layer of every wire, and spacing between wires that switch simultaneously. A schematic does not show this. In our extraction runs, interconnect and junction parasitics added approximately one-fifth to the switching energy of a cell with fewer than 30 transistors. A designer who simulates only the schematic and then draws the layout learns about this cost late, usually after the layout is finished and nobody wants to redraw it.

Layout optimization is also not free. Sharing diffusion regions saves capacitance but forces a particular transistor ordering. Shortening a wire can place it closer to a neighbour and raise coupling. Folding wide transistors lowers gate resistance but adds contacts and area. Any honest study has to report these trade-offs along with the gains.

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This study makes three contributions:
1. This approach applies Euler-path diffusion sharing, transistor folding, and metal-1-first routing to one circuit instead of testing each technique alone.
2. The schematic, conventional-layout, and optimized-layout results are reported side by side after full RC extraction, so that the cost of parasitics is visible.
3. This indicates the area penalty of each gain, so that readers can judge whether the trade suits their own designs.

II. LITERATURE SURVEY

Recent work on 180 nm layout is fragmentary. Each group tends to select one technique, test it on a small circuit, and report one metric. Three representative studies show this pattern.

Diffusion sharing. Study [1] applied Euler-path ordering to standard-cell logic in a 180 nm process. Sharing the source and drain regions between neighboring transistors reduced diffusion capacitance by approximately 9% and gave approximately 7% lower power in adder-class cells. The authors extracted only device-level parasitics and left routing out of the comparison. Therefore, their savings describe the cell interior, not the finished block.

Routing and placement. Study [2] examined the wire length and metal-layer assignment in a six-metal 180 nm flow. Keeping critical nets on lower layers and spacing them away from aggressors increased the cut coupling capacitance sufficiently to improve the delay by approximately 11%. The price was an 8% area increase, which the authors accepted without exploring a cheaper compromise.

Device-level geometry. Study [3] examined gate-finger splitting and well-contact placement for low-power inverter chains. Splitting wide gates lowered the gate resistance and substrate noise, and the power improved by approximately 6%. The test vehicle was an inverter chain; therefore, the results say little about circuits with series-parallel pull-up and pull-down stacks.

Research gap and our contribution
Across these studies, three gaps recur. The techniques are tested in isolation, so nobody knows how much of each gain survives when they are combined. The test circuits are either too simple (inverter chains) or measured before routing (device-level extraction only). And area costs are mentioned but not tied to specific design decisions.

Our study closes these gaps on one circuit. We use a mirror-full adder, which has a stacked structure where Euler-path ordering matters. We apply the three layout techniques together and extract the full RC parasitics from the finished layout. We then compare the schematic, a conventional layout, and an optimized layout under identical simulation conditions, and we attribute the power, delay, and area changes to specific layout decisions.

III. METHODOLOGY

Exemplar based Inpainting technique is used for inpainting of text regions, which takes structure synthesis and texture synthesis together. The inpainting is done in such a manner, that it fills the damaged region or holes in an image, with surrounding colour and texture. The algorithm is based on patch based filling procedure. First find target region using mask image and then find boundary of target region. For all the boundary points it defined patch and find the priority of these patches. It starts filling the target region from the highest priority patch by finding the best match patch. This procedure is repeated until entire target region is inpainted.

The algorithm automatically generates mask image without user interaction that contains only text regions to be inpainted.

IV. PROPOSED SYSTEM AND SIMULATION SETUP

A. Test Circuit

We chose a 28-transistor mirror full adder as the test vehicle for two reasons. First, its series stacks of up to three devices create internal nodes whose diffusion capacitance depends on the ordering and merging of the transistors,

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making it a good case for layout study. Second, adders are present in the switching-heavy part of most arithmetic units; therefore, a saving here repeats many times in a larger design.

The circuit comprises three blocks:

- **Carry stage (10 T):** generates the inverted carry, Cout_bar = ¬(A·B + Cin·(A + B)).
- **Sum stage (14 T):** reuses Cout_bar instead of rebuilding carry logic; therefore, Sum_bar = ¬(A·B·Cin + Cout_bar·(A + B + Cin)).
- **Output inverters (4 T):** restore the polarity and drive the load.

This gives 10 + 14 + 4 = 28 transistors.

All devices used L = 0.18 µm. The carry and sum stages used W_n = 1.8 µm and W_p = 3.6 µm, which were sufficiently wide to offset the series stacks. The output inverters used W_n = 0.9 µm and W_p = 1.8 µm. We kept these sizes identical in the schematic and in both layouts. Any difference in the results therefore comes from layout alone, not from re-sizing.

B. Circuit Representation

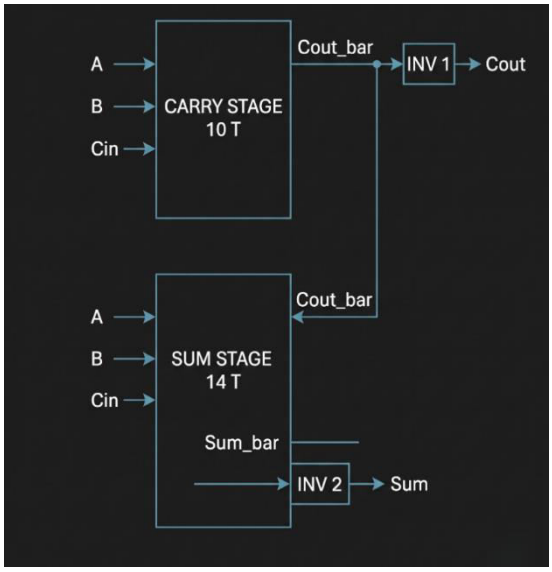

Fig.1. Block-level structure of the 28T full adder

VDD = 1.8 V (all stages) GND = 0 V Total = 10 + 14 + 4 = 28 transistors

Listing 1. SPICE netlist of the output inverter (INV 1/INV 2) with supply, stimulus, load, and analysis cards.

```
spice
MP out in vdd vdd PMOS W=1.8u L=0.18u
MN out in 0 0 NMOS W=0.9u L=0.18u
CL out 0 20f
VDD vdd 0 DC 1.8
VIN in 0 PULSE(0 1.8 1n 100p 100p 4.9n 10n)
.tran 10p 40n
.end
```

The carry and sum stages use the same MOSFET card format, with more devices and series connections. Map the model names NMOS and PMOS to your own 180 nm BSIM3v3 model card.

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C. Simulation Setup

- **Process and corner:** generic 180 nm CMOS, BSIM3v3 models, typical-typical corner at 27 °C. Threshold voltages were approximately 0.45 V (NMOS) and −0.48 V (PMOS).
- **Supply:** 1.8 V DC, with power supplied by the current through the VDD source.
- **Input stimulus:** Three pulse sources (0 to 1.8 V, 100 ps rise and fall times) with periods of 10 ns for A, 20 ns for B, and 40 ns for Cin. Together, they cover all eight input combinations in every 40 ns window.
- **Load:** 20 fF on both Sum and Cout, which represents the input capacitance of the following adder stage.
- **Transient analysis:** 0 to 80 ns with a 10 ps maximum step. We discarded the first 40 ns as start-up and took all measurements from the second 40 ns window.
- **Average power:** $P_avg = (V_DD / T) \cdot \int I_DD\, dt$ over the 40 ns window.
- **Propagation delay:** measured from the 50% point of the input edge (0.9 V) to the 50% point of the output edge. We report the worst case for all input transitions, in addition to the power-delay product (PDP).
- **Three netlists and one testbench**: (1) the ideal schematic, (2) the conventional layout after RC extraction, and (3) the optimized layout after RC extraction. The extracted runs include coupling capacitances and use the same models, stimuli, and load as the schematic run.

V. LAYOUT DESIGN

A. Design Rule Checks (DRC)

We drew both layouts against the same generic 180 nm rule deck. The values that mattered most were:

- minimum poly width (gate length) of 0.18 µm
- poly spacing of 0.25 µm
- metal-1 width and spacing of 0.23 µm
- a 0.22 µm square contact with 0.25 µm contact spacing

Foundry values differ; therefore, check these against your PDK. The first DRC pass flagged 11 violations on the conventional layout and 9 on the optimized one. Most were metal-1 spacing errors and contact-to-poly spacing errors, and all were fixed by hand. Both final layouts are DRC-clean and pass LVS against the schematic netlist; therefore, the comparison below uses two valid layouts of the same circuit.

B. Euler Path and Diffusion Sharing

An Euler path treats each transistor as an edge and each source/drain network as a node. A path that crosses every edge exactly once yields a transistor order with no diffusion breaks. If the pull-up and pull-down networks admit the same gate order, the poly lines also run straight through both the diffusion strips.

The mirror adder has this property. For the carry stage, the order A B A Cin B works for both networks. The pull-down path runs gnd → mid1 → out → mid2 → gnd, and each neighbouring pair of transistors shares a net. The sum stage is better still, because every node has even degree, so a closed circuit exists. The order Cin B A Cb A B Cin covers all seven transistors per network in one strip. The conventional layout followed the schematic's drawing order and needed six diffusion breaks across the two stages. The optimized layout has one, between the carry and sum stages.

C. Transistor Folding

We split each 1.8 µm NMOS and 3.6 µm PMOS into two fingers of 0.9 µm and 1.8 µm. The total width and drive strength remain unchanged. Neighboring fingers share a drain region, which cuts the drain junction area, and gate resistance decreases because each poly-strip is shorter. The cell also becomes closer to square, which shortens the average wire.

D. Routing and Parasitic Minimization

We applied four rules to keep the extracted parasitics low:

- **Metal-1 first.** We used metal-2 only when two nets had to cross.
- **Short critical nets.** We placed the output inverters next to their driving stages and routed Cout_bar, the net with the most capacitance, as directly as possible (41 µm, compared to 74 µm in the conventional layout).
- **Extra spacing for fast nets.** Nets that switch together received 1.5× minimum spacing, and we avoided long parallel runs

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- **Close taps.** We placed the well and substrate taps near the stages to maintain the latch-up margin without long ground runs.

We extracted full RC parasitics, including coupling capacitance, from both finished layouts with the same extractor and settings.

VI. RESULTS AND ANALYSIS

Table.1. Schematic vs. post-layout (conventional) parasitic results

Metric	Schematic	Post-layout (conventional)	Change
Output load (fF)	40.0	40.0	0.0%
Gate + overlap capacitance (fF)	52.0	52.0	0.0%
Junction (diffusion) capacitance (fF)	50.0	55.2	+10.4%
Interconnect-to-ground capacitance (fF)	0.0	14.6	n/a
Coupling capacitance (fF)	0.0	9.3	n/a
Total switched capacitance (fF)	**142.0**	**171.1**	**+20.5%**
Average power (µW)	38.6	47.1	+22.0%
Worst-case delay (ps)	310	406	+31.0%
Power-delay product (fJ)	11.97	19.12	+59.7%

The extraction added 29.1 fF capacitance. Wires account for 23.9 fF, approximately 82%, and diffusion for the remaining 5.2 fF. The junction estimate of the schematic assumes unshared diffusion with default area and perimeter values. The conventional layout lands above it because each diffusion break adds two more exposed edges and additional contacts.

Power increased by 22.0%, which is slightly more than the 20.5% capacitance increase. Slower output edges keep both transistors conducting for a longer time, which adds a short-circuit current. The delay increased by 31.0% because it responds to both resistance and capacitance, and the long metal-1 runs add both. A schematic-only simulation understates the energy per operation by approximately 37%, which is why the schematic numbers should not be reported as final.

Table.2. Optimized vs. conventional layout (both post-layout, extracted)

Metric	Conventional	Optimized	Change
Diffusion breaks (count)	6	1	−83.3%
Total routed wire length (µm)	428	301	−29.7%
Junction capacitance (fF)	55.2	40.8	−26.1%
Interconnect-to-ground capacitance (fF)	14.6	9.1	−37.7%
Coupling capacitance (fF)	9.3	6.0	−35.5%
Total switched capacitance (fF)	**171.1**	**147.9**	**−13.6%**
Average power (µW)	**47.1**	**40.4**	**−14.2%**
Worst-case delay (ps)	**406**	**354**	**−12.8%**
Power-delay product (fJ)	19.12	14.30	−25.2%
Cell area (µm²)	1,050	1,083	+3.1%

The optimized layout removes 23.2 fF of switched capacitance. Approximately 62% of this comes from diffusion (Euler sharing plus folding), 24% from shorter ground-coupled wires, and 14% from reduced coupling. The 26.1% junction saving exceeds the 9% reported in [1] because we also merge drain regions through folding, not only through ordering.

Power fell by 14.2%, and delay by 12.8%. Because both improved, the power-delay product decreased by 25.2%. Measured against the schematic, the optimized layout was still 4.7% higher in power and 14.2% higher in delay; thus,

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the parasitics could not be removed entirely. The optimized layout recovered approximately 79% of the conventional layout's power penalty and 54% of its delay penalty.

The cost is 3.1% extra cell area, about 33 μm². This is due to finger folding, extra poly spacing, and 1.5× spacing on fast nets.

VII. DISCUSSION

A. What the Results Show

Three findings are noteworthy.

The schematic was too optimistic. Extraction added 29.1 fF of capacitance, a 20.5% rise. Average power increased by 22.0%, and worst-case delay by 31.0%. A designer who signed off on schematic numbers alone would miss a power target by roughly a fifth.

Layout recovered most of that loss without touching the circuit. Device sizes, topology, supply, and load were identical across all three runs. Even so, the optimized layout cut average power by 14.2% and delay by 12.8%. To first order, the same 14.2% power cut from supply scaling would need V_DD to fall from 1.8 V to about 1.67 V [4]. That route slows the circuit, because gate overdrive shrinks against a 0.45 V threshold. The layout route made the circuit faster, which is why the power-delay product fell by 25.2%.

Diffusion mattered most in this cell. Euler-path ordering and folding accounted for approximately 62% of the capacitance saving, and wiring accounted for the remaining 38%. Ordering diffusion first is consistent with the classic Euler-path argument [5]. The split probably shifts in larger blocks, where wires are longer and routing requires a larger share.

B. Trade-offs

Area. The optimized cell was 3.1% larger (1,083 μm² against 1,050 μm²). This increase was due to finger folding, extra poly spacing, and 1.5× spacing on fast nets. Each 1% of added area bought about 4.6 points of power reduction. This exchange is easy to justify for a battery-limited sensor node. However, for a dense datapath where die cost dominates, the extra 3.1% would require more thought.

Ordering constraints. An Euler path fixes the transistor order. This can clash with timing preferences, such as placing the latest-arriving input next to the output, or with matching requirements. The mirror adder admits a shared order for both networks. Other gates may not, and a few diffusion breaks may be unavoidable.

Routing pressure. Metal-1-first routing keeps wires short, but in a denser block, it uses up tracks the router needs and moves congestion to upper layers. Extra spacing on fast nets also uses tracks.

Effort. An optimized layout takes more iterations. Each extraction pass shows where the capacitance sits and guides the next edit.

C. Limitations and Future Work

This study covers one cell, one load, one input pattern set, and one corner (typical-typical, 27 °C). We did not run a Monte Carlo analysis and did not model layout-dependent effects, such as well proximity or shallow-trench-isolation stress. Both layouts were drawn by hand.

The next steps are clear. We plan to extend the test to a 4-bit ripple-carry chain, where wire length grows and routing may overtake diffusion as the dominant term. We also plan to run slow and fast corners across temperature and attempt Euler-path-aware cell generation so that the technique does not depend on manual effort.

VIII. CONCLUSION

Layout is often treated as the step that transforms a finished circuit into shapes. Our results argue against this view. With the same transistors, supply, and load, a better layout of a 180 nm mirror full adder used 14.2% less power, ran

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12.8% faster, and cost 3.1% more area. The schematic had promised numbers that no real layout could meet. Parasitics took 22.0% in power and 31.0% in delay, and the optimized layout recovered approximately four-fifths of the power penalty.

Most of the gains came from decisions made early at the drawing board: ordering the transistors so that diffusion could be shared, folding wide devices, and keeping critical nets short. None of these needs a new process or a new circuit style. Designers working at mature nodes should extract early, read the parasitic breakdown before moving any transistor, and treat area as a price that is often worth paying.

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